

# Engineering Fundamentals Exam

## Study Guide For Electrical Engineering Exam



## ***COPYRIGHT NOTICE***

Copyrights © 2014 National Center for Assessment in Higher Education (QIYAS) and Saudi Council of Engineers (SCE) Unless stated otherwise, copyright in this report (including content and design) is owned by the National Center for Assessment in Higher Education (QIYAS) - Riyadh – Saudi Arabia. EXCEPT with the expressed written permission from QIYAS, you may not reproduce, use (in particular for academic or commercial purposes), store in a retrieval system, adapt, modify, communicate to the public or photocopy any part of this report.



## 1. Objectives

The aim of this manual is to provide guidelines for the examinees about the exam structure, timing, percentage of question coverage and distribution among various topic areas. In essence, the manual represents the bridge between the developed Electrical Engineering Standards and the actual phrased questions, which constitute the tests to be administered. It is designed to familiarize the examinees with the test questions formats and contents.

## 2. Contents

This study guide contains essential information for the examinees. Specifically, the following topics are presented in this manual:

- Exam structure, exam schedule and organization, exam type, eligibility for exam, and exam rules
- Organization of the exam framework
- Table of Specifications which includes an overview of the table, its structure and contents
- Sample of questions and solutions for the Electrical Engineering discipline

## 3. Exam Structure

The exam is conducted in two sessions and the duration of each session is 3 hours.

### 3.1 General Engineering Exam

The first session covers the General Engineering topics. These include the following fourteen topics:

1. Mathematics
2. Probability and Statistics
3. Computer Literacy
4. Statics and Dynamics
5. Chemistry
6. Thermodynamics



7. Fluid Mechanics
8. Materials Science and Engineering
9. Electricity and Magnetism
10. Engineering Drawing
11. Engineering Economics
12. Project Management
13. Ethics
14. General Skills
  - a. Use analytical thinking (logical deductions, statements and assumptions, cause and effect, verbal reasoning, analyzing arguments, statements and conclusions, break a complex problem into smaller problems and solve them)
  - b. Use effective communication in writing, orally, and graphically
  - c. Work cooperatively with other team members to deliver the required outcomes
  - d. Set goals and ways for personal development
  - e. Strive for ways to resolve conflicts while being sensitive to others opinions
  - f. Be able to use time and available resources in an efficient way
  - g. Recognize and interpret environmental, social, cultural, political and safety considerations in engineering solutions.
  - h. Recognize decision making process
  - i. Recognize major engineering concepts outside the discipline.
  - j. Interpret uncertainties in measurements and calculations
  - k. Analyze and interpret data
  - l. Apply evaluation criteria and contemporary knowledge to select the optimum design from alternative solutions



### 3.2 Engineering Discipline Exam

The second session covers the Engineering Standards and is based on topics associated with one of the following engineering disciplines:

<i>Code</i>	<i>Discipline</i>
CE	Civil Engineering
CHE	Chemical Engineering
EE	Electrical Engineering
IE	Industrial Engineering
ME	Mechanical Engineering
SE	Structural Engineering

## 4. Exam Implementation

The exam consists of two sessions:

- The first session consists of General Engineering Exam. The total duration of this session is 3 hours with a total number of 90 questions.
- The second session consists of Engineering Discipline Exam. This session consists of 50 questions with a total time of 3 hours.

## 5. Exam Type

The exam is initially paper-based and will become computer based in a later stage. The exam, in both sessions, is of a multiple choice type where each question has four choices for the answer. There is no negative marking for wrong answers.

## 6. Eligibility for the Exam

Bachelor degree holders in an Engineering discipline i.e., Chemical Engineering, Civil Engineering, Electrical Engineering, Industrial Engineering, Mechanical Engineering, and Structural Engineering.



## 7. Exam Rules

- Books, lecture notes, or any type of materials are not allowed in the exam. Necessary reference sheets, monographs, equations, relevant data from codes will be provided in the exam.
- Calculators approved by Exam authorities are allowed.
- Admission in the examination center will be only through authorized admission card
- Examinees are subjected to all the rules and procedures applied by National Center for Assessment in Higher Education (Qiyas)

## 8. Organization of the Exam Framework

The core topics constitute the basis of this Engineering Exam. Indicators are used to describe the knowledge to be tested in each topic. Each of these indicators is further subdivided into three major levels following the recent Bloom's taxonomy of learning levels (Remembering and Understanding; Applying and Analyzing; and Evaluating and Creating).

### Example

<b>Topic:</b>	<b>T2: Power</b>
<b>Indicator:</b>	<b>EE-T2-02</b> Model and calculate parameters of transmission lines
<b>Learning Level:</b>	Applying and Analyzing (AA)

## 9. Table of Specifications

### 9.1 Overview

The Table of Specifications is a map which facilitates the transformation of the Engineering Standards for each Topic Area into balanced and coherent question sheets to be used in the proposed Exam. The Table of Specifications is essentially a tableau structure which distributes, vertically, the exam Questions among various Topic Areas in accordance with the applicable Engineering Standards and, horizontally, over various Learning Levels (Remembering and Understanding, Applying and Analyzing, Evaluating and Creating).



## 9.2 Structure and Contents

The table below constitutes the Table of Specifications for the Electrical Engineering Discipline. The Table of Specifications contains the following columns:

### 9.2.1 Topic Area

These are the widely recognized Topic areas, which are covered in the Electrical Engineering Discipline, namely:

1. Electrical circuits
2. Power systems
3. Electromagnetics
4. Control systems
5. Communications
6. Signal Processing
7. Electronics
8. Digital systems
9. Computer systems

### 9.2.2 % of Test

This column summarizes the total percentage (of the total test) allocated for each Topic Area.

### 9.2.3 Suggested Number of Questions

This column indicates the number of questions to be allocated for each Engineering Standard. The total number of questions per test conforms to the general guidelines which govern the total duration of the test. In the present case, 50 questions are included in each Discipline.

### 9.2.4 Engineering Standards

This column lists the Engineering Standards to be addressed under each Topic Area.

Standards are coded **EE-TJ** (where **EE** denotes the Electrical Engineering Discipline, **TJ** denotes the Topic Number **J**), whereas the Indicators are coded **EE-TJ-K** (where **K** denotes the Indicator number).

For example: **EE-T2-5** is for the question in Electrical Engineering (EE) that represents Topic 2 (Power Systems) and Indicator 5.



### 9.2.5 Assigned Allocations among Learning Levels

The three sub-columns (Remembering and Understanding, Applying and Analyzing, and Evaluating and Creating) under this main column specify the question distribution for the Topic among the three Learning Levels. For example, for the Power (EE-T2), there are two questions assigned to Learning Level **RU**, four questions for **AA** and one question for **EC**.

It is to be noted that the Learning Levels used in the Table of Specifications represent the so-called cognitive levels/processes (levels of thinking) in the revised Bloom's taxonomy. Every two consecutive Learning Levels in Bloom's are combined as one level here.

It is also important to note that the distribution of questions among various Topic Areas follows a careful and rigorous question allocation process, which ensures that appropriate relative levels of coverage are maintained for the various Learning Levels. In the Electrical Engineering Discipline, the distribution of questions (for all Topic Areas) among the three Learning Levels is 15 questions (30%) for Remembering and Understanding, 25 questions (50%) for Applying and Analyzing, and 10 questions (20%) for Evaluating and Creating.



## Table of Specifications for Electrical Engineering Exam

Topic Code	Topic Area	No. of Questions	(% of Exam	Engineering Standards	Assigned Allocations of Questions among Learning Levels		
					RU	AA	EC
T1	Circuits	8	16%	EE-T1	3	4	1
T2	Power	7	14%	EE-T2	2	4	1
T3	Electromagnetics	3	6%	EE-T3	1	1	1
T4	Control Systems	5	10%	EE-T4	1	3	1
T5	Communications	5	10%	EE-T5	2	2	1
T6	Signal Processing	4	8%	EE-T6	1	2	1
T7	Electronics	7	14%	EE-T7	2	3	2
T8	Digital Systems	6	12%	EE-T8	1	4	1
T9	Computer Systems	5	10%	EE-T9	2	2	1
<b>Total</b>		<b>50</b>	<b>100%</b>		<b>15 (30%)</b>	<b>25 (50%)</b>	<b>10 (20%)</b>



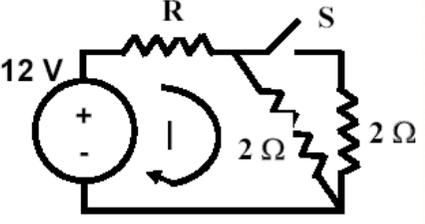
## 10. Sample Questions

A sample of questions is shown in the following tabular format in accordance with the following instructions.

1. For Learning Levels
  - RU for Remembering and Understanding
  - AA for Applying and Analyzing
  - EC for Evaluating and Creating
2. References sheets are denoted in the last column of the Table



### Table of Sample Questions

Q. No.	Topic Area	Standard Code	Learning Level	Question Statement (Answer's Choices)	Answer	Expected Time (min)	supplied Reference
1	Circuits	EE-T1-01	RU	<p>The current (I) flowing through the circuit shown with Switch (S) open is 4A. The value of current (I), in Ampere, with S closed is:</p> <p>A) 2 B) 3 C) 6 D) 12</p> 	C	2.5 – 3	Reference #1
2	Power	EE-T2-08	AA	<p>A transformer of primary voltage 220 V and turns ratio of 11:1. The secondary of the transformer is connected to a 30 Ω inductive reactance in series with a load resistance (R). If the current flowing in (R) must not be below 0.4 A. Then the value of (R) is:</p> <p>A) At least 40 Ω B) At most 40 Ω C) Exactly 20 Ω D) Exactly 50 Ω</p>	B	3 – 4	Reference #2

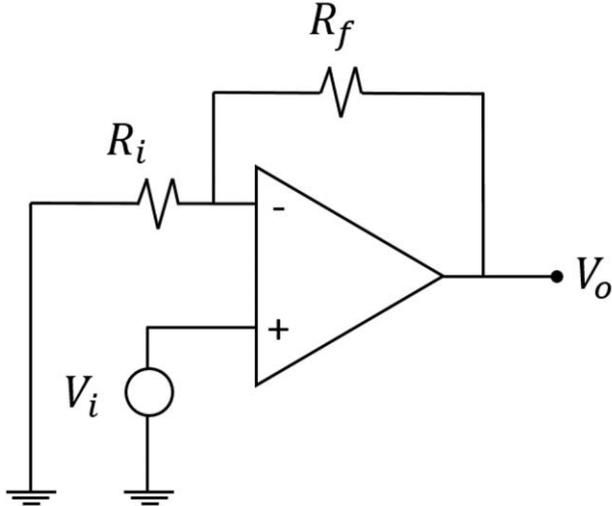


3	Electromagnetics	EE-T3-01	AA	<p>A magnetomotive force was produced in a coil wrapped around a core of an iron-silicon alloy having the magnetizing curve shown in Figure.1, Reference #3. The coil has 10 turns and carrying current of 4 A. If the produced flux passes through an effective cross-sectional area of 2.2 cm<sup>2</sup>. If the magnetic field strength is 10 A/m, then the reluctance of the core is about:</p> <p>A) 200,000 Amp-Turn/Wb  B) 5 μWb/ Amp-Turn  C) 200 Amp-Turn/Wb  D) 5000 μWb/ Amp-Turn</p>	A	4.5 – 5	Reference #3
4	Control systems	EE-T4-03	AA	<p>The steady-state value of the response for an engineering system having a unit step input <math>u(t)</math> and output <math>y(t)</math>, and governed by the differential equation is:</p> $\frac{d^3y}{dt^3} - 4\frac{d^2y}{dt^2} + \frac{dy}{dt} - 2y = 0.1\frac{du}{dt} - 0.5u$ <p>A) 1  B) 0.5  C) 0.25  D) 0</p>	C	3 – 3.5	Reference #4



5	Communication	EE-T5-01	RU	<p>A simple form of AM demodulator consists of:</p> <p>A) Diode in series with a series resistance-capacitance</p> <p>B) Diode in series with a parallel resistance-capacitance</p> <p>C) Diode in parallel with a series resistance-capacitance</p> <p>D) Diode in parallel with a parallel resistance-capacitance</p>	B	1.5 – 2	None
6	Signal processing	EE-T6-05	EC	<p>In an application of Discrete Fourier Transform (DFT), in order to avoid aliasing phenomenon for a forcing function <math>F(t)</math> given by <math>F(t) = \sum_{n=0}^7 10 \times \sin(2\pi n t)</math>, the minimum number of sample data points must be:</p> <p>A) 8</p> <p>B) 16</p> <p>C) 24</p> <p>D) 48</p>	B	1 – 1.5	None



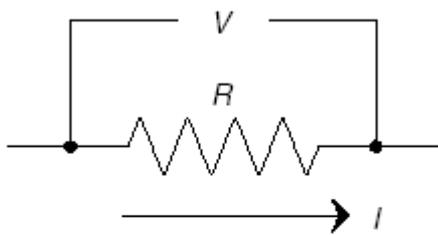
7	Electronics	EE-T7-05	AA	<p>The absolute value of the gain factor for the operational amplifier circuit shown, given <math>R_i = 4.7 \text{ k}\Omega</math> and <math>R_f = 10 \text{ k}\Omega</math>, is approximately:</p>  <p>A) 1          B) 3          C) 5          D) Greater than 5</p>	B	1.5 – 2	Reference #7
---	-------------	----------	----	---	---	---------	--------------



8	Digital systems	EE-T8-07	AA	<p>In a logic gate, power dissipation is calculated as:</p> <ul style="list-style-type: none"> <li>A) Product of average supply current and dc supply voltage</li> <li>B) Product of average supply current and ac supply voltage</li> <li>C) Product of peak current and dc supply voltage</li> <li>D) Product of peak current and ac supply voltage</li> </ul>	A	1 – 1.5	None
9	Computer systems	EE-T9-09	EC	<p>Assigning a memory address to each Input/Output (I/O) device in the computer system is performed using a technique called:</p> <ul style="list-style-type: none"> <li>A) Dedicated I/O</li> <li>B) Ported I/O</li> <li>C) Memory-mapped I/O</li> <li>D) Wired I/O</li> </ul>	C	1 – 1.5	None



## Reference #1

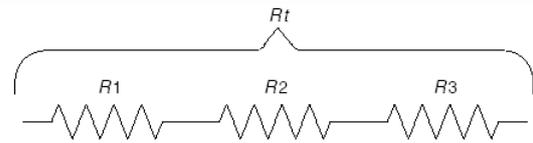


$$V = I \cdot R$$

$$I = \frac{V}{R}$$

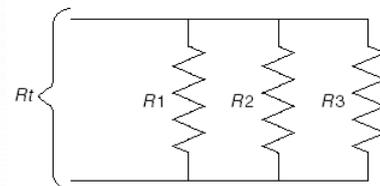
$$R = \frac{V}{I}$$

Ohm's Law



$$R_t = R_1 + R_2 + R_3$$

Series connection



$$\frac{1}{R_t} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}$$

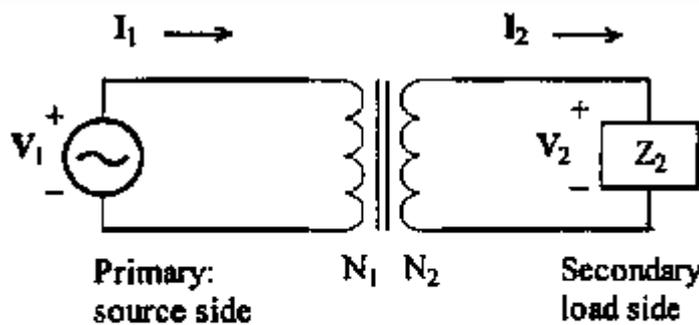
Parallel connection

Resistor		$Z_R = R + 0j$
Capacitor		$Z_C = 0 + 1/j\omega C$
Inductor		$Z_L = 0 + j\omega L$

Impedance of Basic Electrical Components

## Reference #2

Ideal Transformer

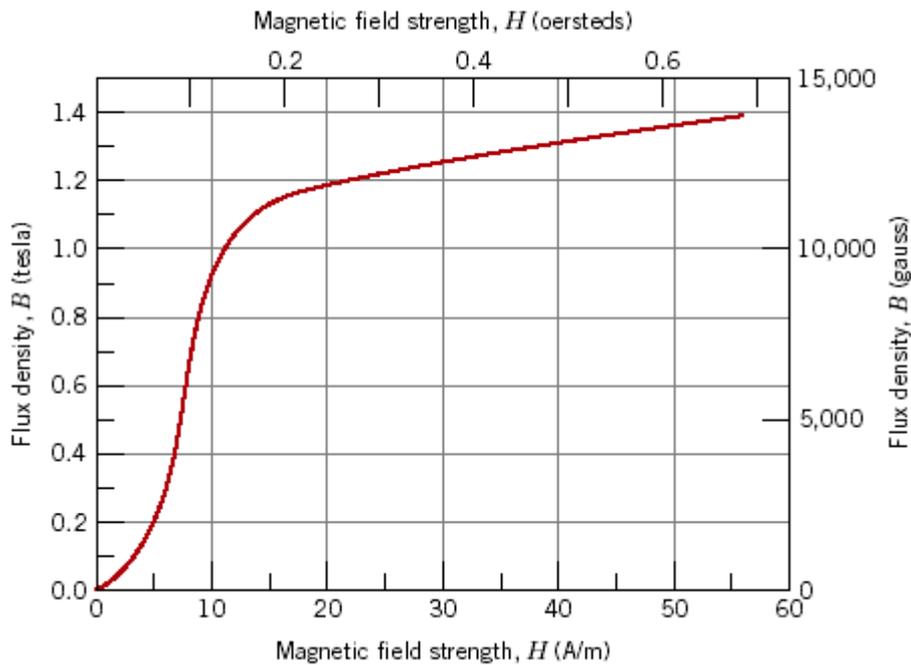


Voltage Transformation:  $\frac{V_1}{V_2} = \frac{N_1}{N_2} = \frac{I_2}{I_1}$



### Reference #3

Figure 1



(Courtesy of [phys.thu.edu.tw/~hlhsiao/mse-web](http://phys.thu.edu.tw/~hlhsiao/mse-web))

### Reference #4

Final Value Theorem:

$$\lim_{t \rightarrow \infty} f(t) = \lim_{s \rightarrow 0} sF(s)$$

$\mathcal{L}$  : denotes Laplace Transform

$$\mathcal{L} \left[ \frac{d^n f(t)}{dt^n} \right] = s^n F(s) \quad (\text{with zero initial conditions})$$

$$\mathcal{L}[u(t)] = \frac{1}{s} \quad u(t): \text{unit step input}$$

### Reference #7

$$\left| \frac{V_o}{V_i} \right| = 1 + \frac{R_f}{R_i}$$



## 11. Solution of the Sample Questions

### Question #1:

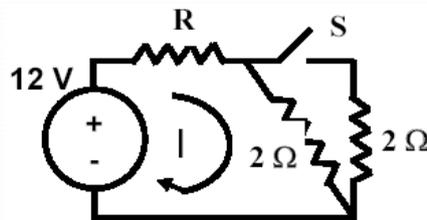
Topic Area: **Circuits**

Indicator: EE-T1-01. Write equations, express and apply fundamental circuit theorems, including KCL, KVL, to simple electrical circuits

#### Question Statement:

The current ( $I$ ) flowing through the shown circuit with Switch ( $S$ ) open is 4A. The value of ( $I$ ) with  $S$  closed is:

- A) 2 A
- B) 3 A
- C) 6 A
- D) 12 A



**Answer:**

C

**Supplied Reference:** Reference #1

**Remarks:**

The objective of this question is to ensure that the examinee can write and interpret KVL to devalue the current flowing in a simple electrical circuit.

**Solution:**

With ( $S$ ) open, the resistance ( $R$ ) is in series with one of the two  $2\ \Omega$  resistances.

Then, the current  $I = 12 / (R + 2) = 4A$ , which gives the value of  $R = 1\ \Omega$ .

When switch ( $S$ ) is closed, the two  $2\ \Omega$  resistances are in parallel and the total equivalent circuit resistance =  $1\ \Omega + (2\ \Omega / 2) = 2\ \Omega$ .

Therefore, the value of  $I$  in this case is  $I = 12\ \text{V} / (2\ \Omega) = 6A$ .



## **Question #2:**

**Topic Area:** Power

**Indicator:** EE-T2-08. *Analyze and assess performance of transformers*

### **Question Statement:**

A transformer of primary voltage 220 V and turns ratio of 11:1. The secondary of the transformer is connected to a  $30 \Omega$  inductive reactance in series with a load resistance (R). If the current flowing in (R) must not be below 0.4 A. Then the value of (R) is:

- A) At least  $40 \Omega$
- B) At most  $40 \Omega$
- C) Exactly  $20 \Omega$
- D) Exactly  $50 \Omega$

### **Answer:**

B

**Supplied Reference:** Reference #2

### **Remarks:**

The objective of this question is to ensure that the examinee can analyze a simple transformer and assess its loading requirement.

### **Solution:**

Let  $V_1$  and  $V_2$  be the primary and secondary transformer voltages, respectively.

$V_1/V_2 = 11/1 = 11$ , where  $V_1 = 220 \text{ V}$  (given)

Therefore the secondary voltage  $V_2 = 220/11 = 20 \text{ V}$ .

When the current flowing in the load resistance is  $I = 0.4 \text{ A}$ , the value of the impedance  $Z$  consisting of the load resistance  $R$  in series with the reactance  $X$  must be:

$$Z = \sqrt{R^2 + X^2} = \sqrt{R^2 + (30)^2} = V_2 / I = 20 / 0.4 = 50 \Omega$$

Which gives a value of  $R = 40 \Omega$

Since the current flowing in the load resistance decreases as the value of the load resistance increases, then for  $I$  to be below 0.4 A, the value of  $R$  must be at most  $40 \Omega$ .



### **Question #3:**

**Topic Area:** **Electromagnetics**

**Indicator:** EE-T3-01. *Model various electrostatics/magnetostatics components and derive the associated basic relationships*

#### **Question Statement:**

A magnetomotive force was produced in a coil wrapped around a core of an iron-silicon alloy having the magnetizing curve shown in Reference Figure.1. The coil has 10 turns and carrying current of 4 A. If the produced flux passes through an effective cross-sectional area of  $2.2 \text{ cm}^2$ . If the magnetic field strength is  $10 \text{ A/m}$ , then the reluctance of the core is about:

- A) 200,000 Amp-Turn/Wb
- B)  $5 \mu\text{Wb/ Amp-Turn}$
- C) 200 Amp-Turn/Wb
- D)  $5000 \mu\text{Wb/ Amp-Turn}$

#### **Answer:**

A

**Supplied Reference:** Reference #3

#### **Remarks:**

The objective of this question is to ensure that the examinee can model a simple coil and derive the associated basic electromagnetic relationships.

#### **Solution:**

From the given magnetizing curve (Reference Figure #1), the value of the magnetic flux density  $B$  corresponding to magnetic field strength value of  $10 \text{ A/m}$  is:

$$B = 0.91 \text{ tesla (Wb/m}^2\text{)}$$

$$\text{The magnetic flux} = B * \text{Cross-sectional area} = 2.2 \times 10^{-4} * 0.91 \approx 2 \times 10^{-4} \text{ Wb}$$

Now, the magnetomotive force is the product of the current flowing in the coil and its number of turns =  $4 * 10 = 40 \text{ Amp-Turn}$ .

The reluctance is defined as the magnetomotive force divided by the flux. Therefore, Reluctance  $\approx 40 / (2 \times 10^{-4}) \approx 20 \times 10^4 = 200,000 \text{ Amp-Turn/Wb}$



## Question #4:

**Topic Area:** Control Systems

**Indicator:** EE-T4-03. *Analyze performance and evaluate steady-state errors of control systems subjected to various input signals*

### **Question Statement:**

The steady-state value of the response for an engineering system having output  $y(t)$  and governed by the differential equation:

$$\frac{d^3y}{dt^3} - 4\frac{d^2y}{dt^2} + \frac{dy}{dt} - 2y = 0.1\frac{du}{dt} - 0.5u$$

With a unit step input  $u(t)$  and output  $y(t)$ :

- A) 1
- B) 0.5
- C) 0.25
- D) 0

### **Answer:**

C

**Supplied Reference:** Reference #4

### **Remarks:**

The objective of this question is to ensure that the examinee can apply controller performance assessment principles to derive the steady-state error in a control system.

### **Solution:**

Taking the Laplace transform of the two sides of differential equation (using the given Reference Table #1), we get:

$$(S^3 - 4S^2 + S - 2) Y(S) = (0.1S - 0.5) U(S)$$

That is, the transfer function is

$$G(S) = Y(S) / U(S) = (0.1S - 0.5) / (S^3 - 4S^2 + S - 2)$$

For a unit-step function (see Reference Table #1),  $U(S) = 1/S$

The steady-state value of the response to a unit-step function is therefore:

$$Y_{ss} = \text{Limit} \{s Y(s)\} \text{ as } s \rightarrow 0 = \text{Limit} \{G(s)\} \text{ as } s \rightarrow 0 = -0.5 / (-2) = 0.25$$



## Question #5:

**Topic Area:** Communications

**Indicator:** EE-T5-01. *Model and apply basic modulation/demodulation concepts, including AM, FM, and PCM*

### **Question Statement:**

A simple form of AM demodulator consists of:

- A) Diode in series with a series resistance-capacitance
- B) Diode in series with a parallel resistance-capacitance
- C) Diode in parallel with a series resistance-capacitance
- D) Diode in parallel with a parallel resistance-capacitance

### **Answer:**

B

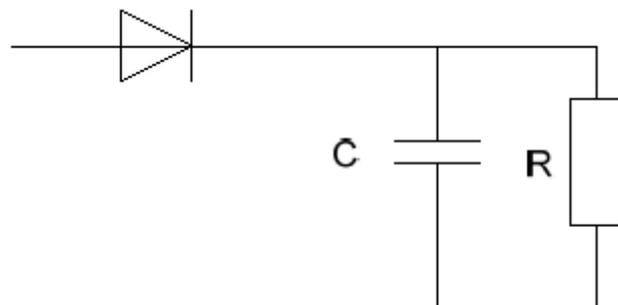
**Supplied Reference:** None

### **Remarks:**

The objective of this question is to ensure that the examinee is aware of the function of filters in the AM demodulation process.

### **Solution:**

A simple form of AM demodulator is the diode detector circuit, which is a non-coherent detector (not synchronized in phase with the transmitter) as shown in the accompanying figure. A low-pass filter (with appropriate time constant) must be connected in series with the diode. The only option which provide such low-pass filtering process is option (B) since the parallel resistance-capacitance constitute a low-pass filter.



## **Question #6:**

**Topic Area:** **Signal Processing**

**Indicator: EE-T6-05.** Apply Fast Fourier Transform (FFT) and Discrete Fourier Transform (DFT) in processing signals

### **Question Statement:**

In an application of Discrete Fourier Transform (DFT), in order to avoid aliasing phenomenon for a forcing function  $F(t)$  given by  $F(t) = \sum_{n=0}^7 10 \times \sin(2\pi n t)$ , the minimum number of sample data points must be:

- A) 8
- B) 16
- C) 24
- D) 48

### **Answer:**

B

**Supplied Reference:** None

### **Remarks:**

The objective of this question is to ensure that the examinee can recognize in practice the conditions and limitations of applying Discrete Fourier Transform to process signals.

### **Solution:**

The number of data points should be at least twice the highest harmonic component present in the (forcing) function, namely 8 for the given function (since 7,6,5,4,3,2,1,0 = n).



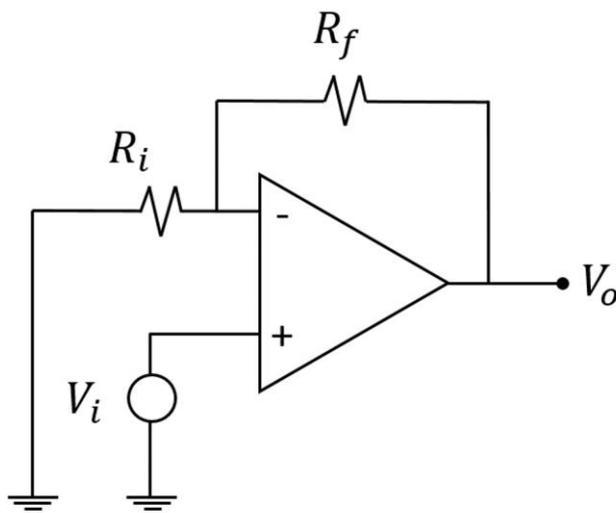
## Question #7:

Topic Area: **Electronics**

Indicator: EE-T7-07. *Apply design concepts to optimize performance of operational amplifiers*

### Question Statement:

The absolute value of the gain factor for the operational amplifier circuit shown, given  $R_i = 4.7 \text{ k}\Omega$  and  $R_f = 10 \text{ k}\Omega$ , is approximately:



- A) 1
- B) 3
- C) 5
- D) Greater than 5

### Answer:

B

Supplied Reference: Reference #7

### Remarks:

The objective of this question is to ensure that the examinee can assess the resulting gain of practical operational amplifier circuits as an important performance criterion.



**Solution:**

As shown in the accompanying figure, the amplifier is non-inverting with the feedback loop closed. The closed-loop gain of the amplifier is given by:

$$\text{Gain} = 1 + (R_f / R_i) = 3.1277$$



## Question #8:

Topic Area: **Digital Systems**

Indicator: EE-T8-10. *Design and assess performance of logic gates and circuits*

### Question Statement:

In a logic gate, power dissipation is calculated as:

- A) Product of average supply current and dc supply voltage
- B) Product of average supply current and ac supply voltage
- C) Product of peak current and dc supply voltage
- D) Product of peak current and ac supply voltage

### Answer:

A

Supplied Reference: None

### Remarks:

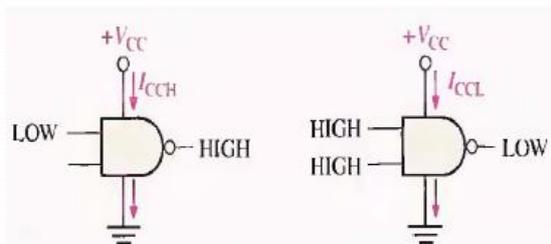
The objective of this question is to ensure that the examinee can evaluate power dissipation in a logic gate as an important design parameter.

### Solution:

As shown in the accompanying figure, the logic gate draws a current  $I_{CCH}$  from the supply when the gate is in the “high” output state and draws a current  $I_{CCL}$  from the supply when the gate is in the “low” output state. Power dissipation in the logic gate is defined as:

$$P_{\text{Dissipation}} = V_{CC} * (I_{CCH} + I_{CCL}) / 2$$

Which is the product of average supply current and dc supply voltage



(Courtesy of [www.uotechnology.edu.iq/dep-eee/lectures/4th](http://www.uotechnology.edu.iq/dep-eee/lectures/4th))



## **Question #9:**

**Topic Area:** **Computer Systems**

**Indicator:** EE-T9-09. *Describe and explain usage and importance of microprocessors in practice*

### **Question Statement:**

Assigning a memory address to each Input/Output (I/O) device in the computer system is performed using a technique called:

- A) Dedicated I/O
- B) Ported I/O
- C) Memory-mapped I/O
- D) Wired I/O

### **Answer:**

C

**Supplied Reference:** None

### **Remarks:**

The objective of this question is to ensure that the examinee can recognize the design features of a practical computer system.

### **Solution:**

Memory-mapped I/O (MMIO) is used to perform input/output between the CPU and peripheral devices in a computer. Memory-mapped uses the same address bus to address both memory and I/O devices – the memory and registers of the I/O devices are mapped to (associated with) address values. So when an address is accessed by the CPU, it may refer to a portion of physical RAM, but it can also refer to memory of the I/O device. Thus, the CPU instructions used to access the memory can also be used for accessing devices. Each I/O device monitors the CPU's address bus and responds to any CPU access of an address assigned to that device, connecting the data bus to the desired device's hardware register. To accommodate the I/O devices, areas of the addresses used by the CPU must be reserved for I/O and must not be available for normal physical memory.



